Drone Based Surveillance Radar

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This report presents the design and validation of a voltage-controlled oscillator (VCO) for a phase-locked loop in a drone-based radar system. A varactor-based tuning method was first modeled and verified in simulation, but showed instability when integrated into the oscillator. An alternative midpoint biasing approach was then implemented, resulting in improved stability and output performance. The final design, including an op-amp control circuit, was tested on hardware and showed good agreement with simulations. This work highlights the importance of considering parasitic effects and system-level behavior in high-frequency oscillator design.

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CHAPTER 1

INTRODUCTION

1.1 Radar Introduction

The project in progress is a drone based short range surveillance radar, meant for air traffic control of multiple delivery drones. The increasing deployment of delivery drones in low-altitude airspace has created new challenges for safe and efficient air traffic control[1;2]. With this increase, there needs to be an increase in safety measures, particularly in urban environments where obstacles, clutter, and dynamic flight paths are common.

The project builds on radar sensing and signal processing principles to detect and track small aerial targets under strict size, weight, and power constraints. Short-range radar operation in low-altitude environments presents challenges such as ground clutter, multipath effects, and small radar cross sections, which require tailored waveform design and processing techniques[3;4]. The integration of compact radar hardware with onboard processing highlights the role of advanced sensing technologies in future UAV traffic management systems, supporting scalable and autonomous control of delivery drone fleets.

1.2 Literature Review

My group is working on the phase-locked loop within the project, I focus specifically on the voltage-controlled oscillator (VCO). In preparation for the phase locked-loop, an important piece of writing is Phase-Locked Loops: Application to Coherent Receiver, written by Alain Blanchard. This text provides a clear introduction to the fundamental operating principles of phase-locked loops, with a strong emphasis on their use in coherent receiver systems such as radar. It discusses loop dynamics, locking behavior, noise performance, and the impact of oscillator stability on system-level performance, making it highly relevant for understanding how the VCO influences the overall PLL behavior in a radar application[5]. Phaselock Techniques by Floyd M. Gardner is another very important book that focuses on the theoretical and mathematical analysis of phase-locked loops, including stability, transient response, and phase noise. This reference is particularly valuable for understanding how VCO parameters such as tuning gain and noise characteristics affect loop performance and locking accuracy[6]. Lastly, as I focused on the VCO, I read the text Design of High-Performance CMOS Voltage-Controlled Oscillators, written by Liang Dai and Rameesh Harjani. This book focuses specifically on the design and implementation of VCOs, covering oscillator architectures, phase noise sources, tuning range, and power consumption, and provides practical design methodologies that are directly applicable to developing a stable, low-noise VCO for use within the PLL[7].

1.3 Problem Statement

The goal of this project is to design and validate a 5.4 GHz voltage-controlled oscillator (VCO) suitable for integration within a phase-locked loop for radar-based applications. The project works with theoretical oscillators and PLL concepts and their practical implementation. Within the team, I am responsible for the VCO subsystem, with a specialized focus on the tuning capabilities. Many existing state-of-the-art solutions prioritize high

integration or wide tuning range while obscuring design trade-offs or degrading phase noise through aggressive optimization[8;7]. This project explicitly addresses these deficiencies by adopting a transparent, noise-aware design methodology that emphasizes physical insight and system-level performance considerations.

1.4 Technical Contribution Statement

The novelty of this project comes from a system-oriented application of well-established RF oscillator design principles, rather than the development of a new oscillator topology. Instead of focusing on creating a fundamentally new circuit, the work emphasizes how an existing Colpitts VCO can be adapted and integrated effectively within a larger phase-locked loop (PLL) system intended for radar applications.

In this context, the VCO is treated as a critical subsystem whose performance directly impacts overall system behavior. Design decisions were not made in isolation, but rather evaluated based on their effect on key system-level metrics such as PLL stability, phase noise, tuning range, and robustness. This approach ensures that the oscillator does not become a limiting factor in the performance of the complete radar system.

A central aspect of this work is the implementation of the VCO tuning mechanism. The primary contribution focuses on developing and evaluating different methods for achieving frequency tunability at 5.4 GHz. This includes:

- The design and consideration of a varactor-based tuning approach, requiring an understanding of device behavior at gigahertz frequencies, as well as the impact of parasitic elements and nonlinearities.
- The development of an op-amp-based interface used to generate and buffer the control voltage from the loop filter, ensuring that the tuning signal is stable and does not introduce additional loading or noise into the system.
- The evaluation of an alternative midpoint biasing technique, which simplifies implementation while still providing sufficient tuning capability within the required operating range.

Particular attention is given to how these elements interact with the rest of the PLL. For example, the sensitivity of the VCO tuning gain directly affects loop dynamics, while noise on the control voltage can translate into phase noise at the output. As a result, the tuning circuitry is designed to minimize unwanted coupling and maintain predictable behavior across the operating range.

Another important aspect of the work is the inclusion of practical, non-ideal effects in the design process. Parasitic resistances, inductances, and component limitations at high frequencies are taken into account to better reflect real-world performance. This helps ensure that the transition from simulation to physical implementation is realistic and does not require significant redesign.

Overall, the contribution of this project lies in the careful integration of the VCO within a larger system, rather than in the invention of new circuit techniques. By focusing on tuning functionality, control interface design, and system compatibility, the work demonstrates a disciplined and practical approach to RF subsystem design. The result is a VCO that meets the required specifications while remaining compatible with the broader PLL and radar system requirements.

CHAPTER 2

PHASE-LOCKED LOOP (PLL) DESCRIPTION

2.1 Phase-Locked Loop (PLL) Objective

The primary goal of this project is to design and implement a phase-locked loop (PLL) operating around 5.4 GHz for a drone-based short-range surveillance radar system. The PLL serves as a stable and low-noise frequency reference for both the transmitter and receiver, which is essential for reliable detection and tracking of multiple delivery drones.

The design focuses on achieving strong frequency stability, reasonably low phase noise, and fast lock times, while remaining compact and power-efficient for UAV deployment. The target operating frequency is approximately 5.4 GHz, with a tuning range of about ± 0.1 GHz to provide flexibility in operation. Key performance metrics include lock stability, phase noise, and tuning capability. These will be evaluated through both simulation and hardware testing to ensure the PLL meets the requirements of a mobile radar system[9;6].

2.2 Overall Challenges

This project presents several technical and personal challenges. On a personal level, one of the main difficulties is gaining familiarity with simulation tools such as Advanced Design System (ADS), which is required for modeling and validating the voltage-controlled oscillator (VCO). Additionally, prior to this course, I had limited exposure to PLL concepts, requiring significant effort to understand their theory, operation, and design considerations.

From a system perspective, integrating a PLL into a drone-based radar introduces challenges related to maintaining frequency stability and low phase noise under strict size, weight, and power constraints[4]. Designing the VCO to meet both tuning range and phase noise requirements, while remaining compatible with the loop dynamics, is particularly demanding[8;7]. Furthermore, testing and validating the PLL in hardware may present additional difficulties, including measurement limitations and discrepancies between simulated and real-world performance.

2.3 Proposed Approach & Solution

Figure 2.1 illustrates the overall radar system architecture. Although the diagram may appear complex at first glance, it can be divided into four main functional groups.

The first group is the antenna subsystem, which is responsible for transmitting and receiving radar signals. Separate transmit and receive antennas are used to reduce self-interference while enabling detection of reflected signals from targets. These reflected signals contain range and velocity information, which can be extracted through time delay and Doppler shift analysis[3;4].

The second group is the microwave subsystem, which handles high-frequency analog signal processing. This includes low-noise amplifiers (LNAs) to boost weak received signals, a power amplifier (PA) to provide sufficient transmit power, a crystal oscillator for frequency reference generation, and band-pass filters to suppress out-of-

band noise. These components work together to maintain signal integrity and spectral purity throughout the RF chain[10].

The third group is the digital signal processing (DSP) subsystem. This section includes analog-to-digital converters (ADCs), lookup tables (LUTs), and processing blocks used to extract range and velocity information from the received signals. A pseudonoise generator is also included to support modulation and signal processing functions.

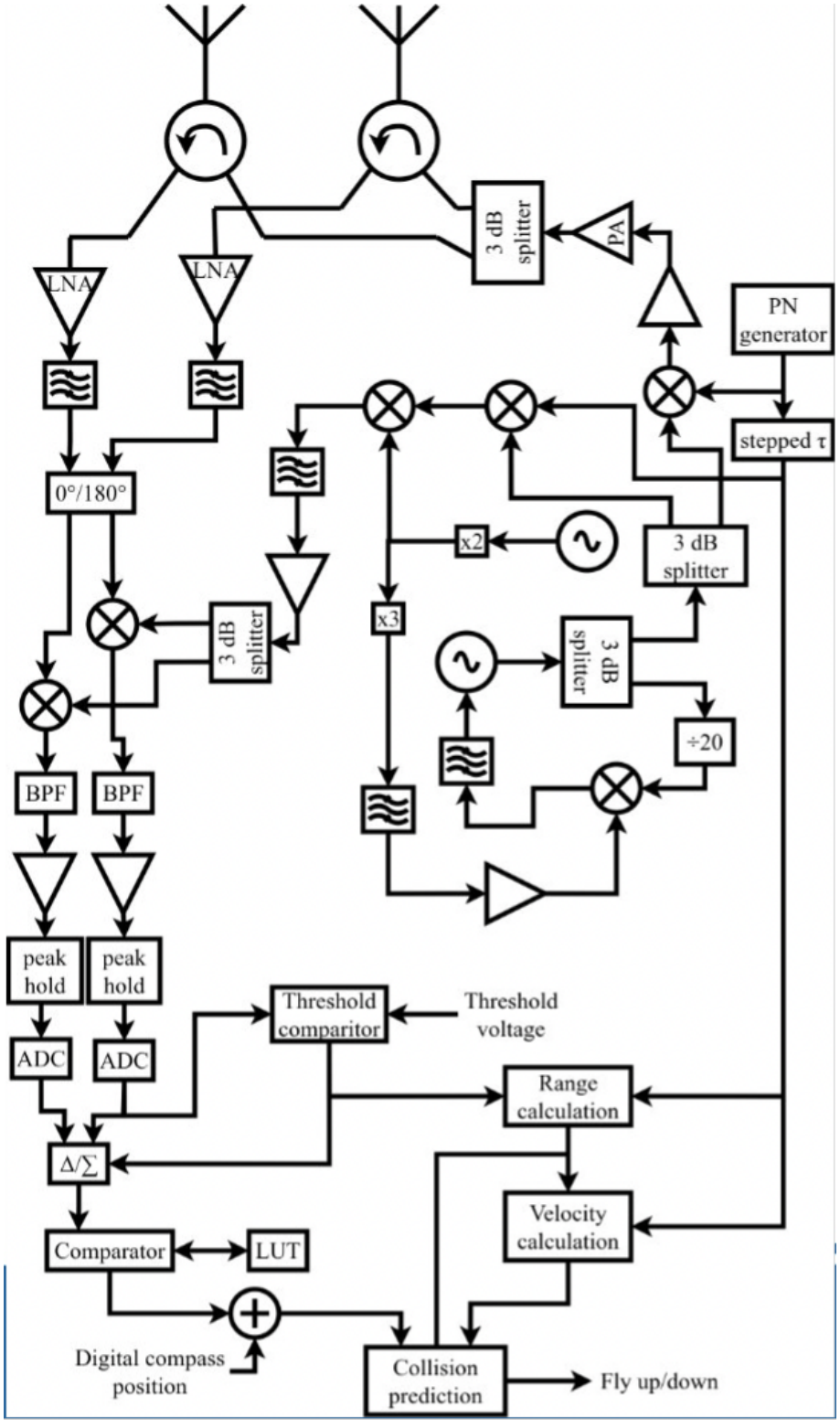

Figure 2.1: Block diagram for the entire radar

Figure 2.2 shows the block diagram of the PLL, which is the focus of this project. In this configuration, a low-frequency reference oscillator is first conditioned through amplification and filtering stages. It is then

compared with a feedback signal derived from the VCO output. The resulting phase error is passed through a loop filter to generate a control voltage, which tunes the VCO and maintains phase and frequency lock. This process allows the PLL to produce a stable 5.4 GHz output while minimizing phase noise and long-term drift [9;6].

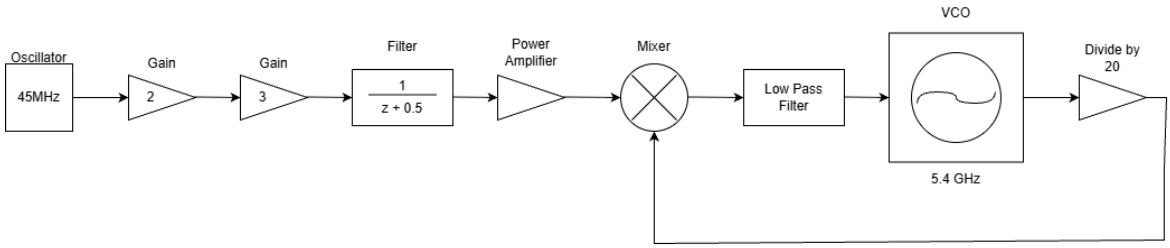

Figure 2.2: Simulink block diagram of the phase-locked loop

2.4 Design Stages

The PLL portion of the project is being developed by a team of five people, with the work divided into four main sections. Referring to Fig. 2.2, the system begins with a 45 MHz crystal oscillator from the microwave group. This signal is first doubled to 90 MHz using a frequency multiplier, and then further multiplied by a factor of three within the PLL to produce a 270 MHz reference signal.

This two-stage multiplication is necessary because the intermediate 90 MHz signal is also used elsewhere in the radar system, as shown in Fig. 2.1. After multiplication, the 270 MHz signal is passed through filtering and amplification stages to ensure sufficient signal quality and amplitude for phase comparison. These stages are handled by one team member.

The reference signal is then fed into a mixer, where it is compared with a feedback signal derived from the VCO output. The feedback path includes a divide-by-20 block, which scales down the high-frequency VCO output to match the reference frequency range required for proper comparison. Another team member is responsible for the design of both the mixer and the divider.

The loop filter, assigned to a third team member, follows the phase detector. Although labeled as a low-pass filter, its role is more specific: it removes high-frequency components from the phase error signal while shaping the loop dynamics to ensure stability and proper locking behavior.

The final stage of the PLL is the VCO, which is being developed collaboratively. One team member focuses on the Colpitts oscillator core, including feedback and start-up conditions. My contribution focuses on the tuning mechanism using a varactor. This involves analyzing how the control voltage affects the effective tank capacitance, tuning range, and frequency sensitivity, while ensuring that the tuning network does not degrade phase noise or interfere with sensitive RF nodes. Together, these efforts ensure that the VCO meets the requirements of both the PLL and the overall radar system.

CHAPTER 3

PROPOSED APPROACH FOR TUNING THE COLPITTS OSCILLATOR

3.1 Principle and Theory of the Varactor-Tuned Colpitts Oscillator

The Colpitts oscillator is a widely used LC oscillator in RF and microwave applications due to its simplicity, frequency stability, and ease of integration. Its basic configuration consists of a transistor or active device, an LC tank circuit formed by an inductor and two series capacitors, and feedback taken from the capacitive divider. The oscillation frequency f_0 is determined primarily by the tank circuit and is given by:

$$f_0 = \frac{1}{2\pi\sqrt{L \cdot C_{\text{eq}}}}, \quad \text{where} \quad C_{\text{eq}} = \frac{C_1 C_2}{C_1 + C_2} \tag{3.1}$$

where L is the inductance and C_1 and C_2 are the capacitors in the Colpitts configuration[10].

Incorporating a varactor diode into the Colpitts oscillator allows the oscillation frequency to be electronically tuned by varying the reverse bias voltage applied to the varactor[7]. The varactor effectively changes the equivalent capacitance C_{eq} in the tank circuit, resulting in a tunable oscillator frequency. The nonlinear voltage-dependent capacitance of the varactor can be modeled using the small-signal approximation:

$$C(V_R) = C_0 \left(1 + \frac{V_R}{V_j}\right)^{-m} \tag{3.2}$$

where C_0 is the zero-bias capacitance, V_R is the reverse bias voltage, V_j is the junction potential, and m is the grading coefficient. The design challenge is to maintain low phase noise and frequency stability across the tuning range[9;6].

For mathematical modeling and simulation, the oscillator can be analyzed using linear small-signal analysis, harmonic balance, or time-domain transient simulations. The behavior of the varactor-tuned Colpitts oscillator can be further studied using circuit simulators such as ADS or SPICE, which allow visualization of oscillation waveforms, frequency spectrum, and tuning characteristics[7].

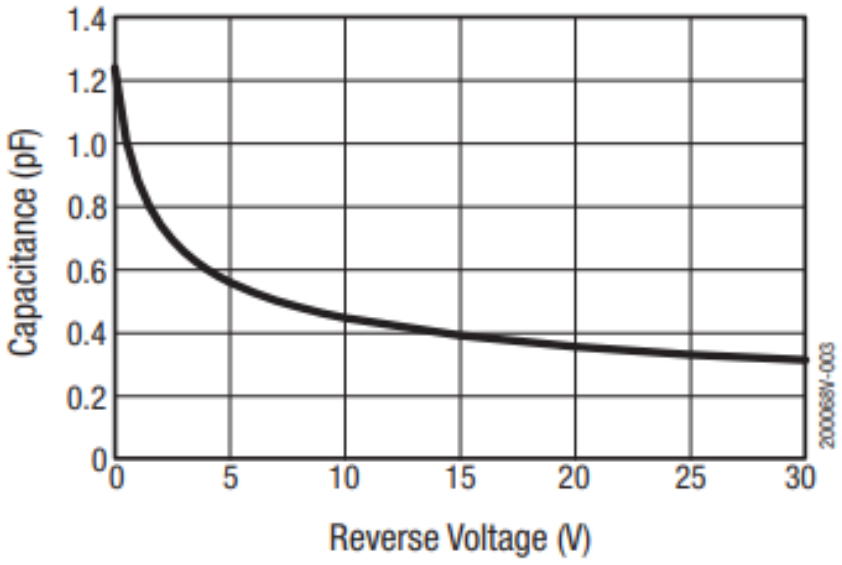

Figure 3.1: Variation of varactor capacitance with reverse bias voltage.[11]

As shown in Figure 3.1, the varactor capacitance decreases nonlinearly with increasing reverse bias voltage. This behavior of the varactor is critical for tuning the Colpitts oscillator, as changes in reverse voltage directly modify the effective capacitance of the tank circuit and consequently the oscillation frequency. Observing this relationship allows for precise design of the oscillator tuning range and analysis of frequency stability across the operating conditions. Future simulation and hardware tests can use this data to validate the expected oscillator response and phase noise performance.

In practical high-frequency implementations such as a 5.4 GHz Colpitts oscillator, the reverse bias voltage applied to the varactor is typically generated through a buffered control stage rather than being applied directly. An op-amp is commonly used to interface the tuning voltage source or loop filter with the varactor diode. The op-amp provides high input impedance to avoid loading the control circuitry and low output impedance to ensure a stable and noise-resilient bias voltage. This is particularly important at microwave frequencies, where even small fluctuations in the control voltage can lead to noticeable frequency deviations. The op-amp output is usually connected to the varactor through an RF choke or high-value resistor, which isolates the RF oscillation from the DC control path while preserving the tuning functionality[8;6].

3.2 Technical Challenges and Issues

At this stage of the project, several technical challenges are anticipated. One major challenge is the accurate modeling of the varactor diode, since its nonlinear voltage-dependent capacitance directly affects the oscillator frequency and tuning linearity. Small variations in the varactor's junction characteristics, temperature dependence, and parasitic series resistance can significantly impact phase noise and frequency stability. According to[7], careful consideration of varactor parameters and layout is critical for achieving low phase noise in compact VCO designs.

Another challenge is predicting and maintaining stable oscillation across the tuning range. Traditional small-signal analysis can approximate behavior, but harmonic balance or transient simulations in ADS or SPICE are often necessary to capture nonlinear effects and verify frequency tuning under different bias conditions[9;12]. Existing state-of-the-art VCO designs mitigate these issues by using optimized tank circuit topologies, high-Q inductors, and feedback techniques to reduce phase noise and sensitivity to component variations[6]. For a UAV-mounted radar system, additional practical constraints include power consumption, size, and environmental robustness, which further complicate the design and testing of the VCO.

An additional challenge arises from the inclusion of the op-amp-based tuning interface between the loop filter and the oscillator. While the op-amp improves control over the varactor bias voltage, it also introduces noise and bandwidth limitations that can degrade overall oscillator performance. At 5.4 GHz, even low-level

voltage noise at the op-amp output can be upconverted into phase noise due to the high tuning sensitivity of the varactor. Therefore, careful selection of low-noise op-amps and proper filtering of the control voltage are essential. Furthermore, the bandwidth of the op-amp must be sufficient to respond to tuning variations without introducing delay or instability, particularly in closed-loop systems such as phase-locked loops. Parasitic effects from PCB layout, including coupling between the RF tank and the control line, must also be minimized to prevent unwanted modulation of the oscillation frequency[9;8].

3.3 Important Design Aspects: Features & Limitations

The primary feature of the chosen approach is the design and integration of a varactor diode tailored for operation within a 5.4 GHz Colpitts oscillator. Rather than relying on an idealized capacitance element, the varactor is selected and modeled based on its voltage-dependent capacitance characteristics and high-frequency performance. Key parameters such as junction capacitance, junction potential, grading coefficient, series resistance, and parasitic inductance must be carefully considered, as they directly influence the effective tank capacitance and thus the oscillation frequency. At microwave frequencies, minimizing series resistance and parasitic inductance is particularly important to preserve the quality factor of the resonant tank and maintain low phase noise.

Using manufacturer datasheet parameters as a starting point, the varactor can be incorporated into ADS through an HSPICE-compatible nonlinear model. This enables analysis of capacitance variation as a function of reverse bias voltage under realistic operating conditions. Parameter sweeps of the control voltage allow for estimation of the achievable tuning range and sensitivity of the oscillator. In addition, proper biasing of the varactor requires the inclusion of an RF choke or high-value resistor to isolate the RF signal from the DC control path, ensuring stable operation of the oscillator.

To support controlled tuning, the varactor bias voltage is provided through an op-amp-based interface connected to the loop filter. The op-amp must be selected to provide low output noise, sufficient bandwidth, and stable operation over the required control voltage range. Its role is to buffer the loop filter output and deliver a well-defined tuning voltage to the varactor without introducing significant loading or distortion. In this context, the noise performance of the op-amp is critical, as fluctuations in the control voltage are directly translated into frequency variations at the oscillator output. As a result, careful filtering and decoupling of the control line are required to suppress unwanted noise contributions.

Part Number	C_{JO} (pF)	V_J (V)	M	C_P (pF)	R_S (Ω)
SMV1405	2.37	0.77	0.5	0.29	0.80
SMV1408	3.89	0.92	0.5	0.21	0.60
SMV1413	8.92	0.87	0.5	0.30	0.35
SMV1430	1.11	0.86	0.5	0.13	3.15

Figure 3.2: SPICE model parameters[11]

However, this approach has several limitations. The varactor datasheet provides only a subset of the parameters required for a complete nonlinear device model, as shown in Fig. 3.2. As a result, certain parameters, particularly those related to high-frequency parasitics and package effects, must be approximated or extracted, which introduces uncertainty into the simulation results. Furthermore, the model does not fully capture temperature dependence, large-signal RF behavior, or layout-induced parasitics, all of which become increasingly significant at 5.4 GHz. Similarly, non-idealities in the op-amp, including finite bandwidth and output noise, are not always fully represented in system-level simulations. Consequently, while the proposed design approach provides a realistic approximation of the oscillator behavior, discrepancies between simulated and measured performance are expected[10;8;7].

3.4 Comparison with State-of-the-art techniques

The simulated capacitance–voltage characteristic of the SMV1405 varactor model, shown in Fig. 3.3, shows the expected decrease in capacitance with increasing reverse-bias voltage, consistent with varactor theory. This trend closely matches the behavior reported in the datasheet measurements, as shown in Fig. 3.1, even though that figure represents the SMV1430 device rather than the SMV1405. Since both devices belong to the same

varactor family, the similarity in trend indicates that the implemented HSPICE model accurately captures the voltage-dependent capacitance behavior required for VCO tuning. This agreement with theoretical expectations and existing solutions confirms the suitability of the modeling approach for use in the proposed design.

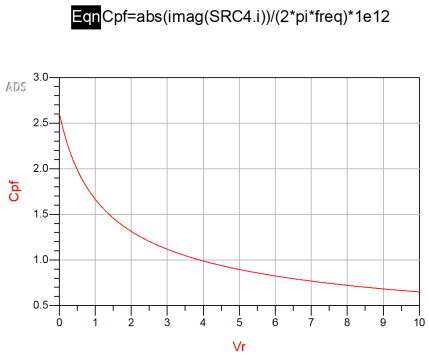

Figure 3.3: Simulated capacitance–voltage characteristic of the SMV1405 varactor model obtained from ADS

3.5 Alternative Techniques

An alternative approach to frequency tuning was ultimately chosen for this design, namely applying the tuning bias at the midpoint of the capacitive divider. This method was selected as a more practical solution within the project constraints, even though varactor-based tuning is generally preferred in high-performance designs.

In the midpoint tuning configuration, the control voltage is applied directly to the node between the two tank capacitors. While this provides a straightforward way to adjust the oscillation frequency, it comes with several trade-offs. This node experiences a large RF voltage swing, so introducing a DC bias requires isolation components such as RF chokes or high-value resistors to prevent RF leakage into the control path. These additional elements introduce parasitic impedances, which load the resonant tank and reduce its effective quality factor (Q), ultimately degrading phase noise performance[8;9].

Another important consideration is that the midpoint node is part of the oscillator's feedback network. Any loading from the biasing circuitry can alter the feedback ratio and loop gain, which may affect both the start-up condition and the steady-state amplitude stability[10]. In addition, the large RF swing at this node increases the likelihood of RF feedthrough onto the tuning line, making the oscillator more sensitive to noise on the control voltage and potentially introducing unintended frequency modulation[6;13].

Although this approach has clear limitations, it offers a relatively simple and robust way to achieve the required frequency tuning range. In contrast, a varactor-based solution requires careful device design and accurate high-frequency modeling, particularly at 5.4 GHz. Developing and validating such a model, and integrating it reliably into the oscillator design, proved to be more difficult than expected within the available time.

For these reasons, midpoint biasing was considered a reasonable compromise at this stage of the design, with the understanding that a varactor-based implementation remains a strong candidate for future improvements.

CHAPTER 4

EXPERIMENTAL DEMONSTRATION

4.1 Design Considerations

The PLL group is broken up into four groups as discussed in Chapter 2, and for testing each group is evaluated using either ADS or KiCad. After circuit-level simulation, the oscillator layout is further analyzed within ADS using its electromagnetic simulation tool (Momentum) to account for layout-dependent parasitics, transmission line effects, and coupling phenomena that are not fully captured in schematic-level simulations, particularly at gigahertz frequencies. This allows for more accurate evaluation of impedance matching and signal integrity within the PCB layout[10]. The finalized layout is then exported as Gerber files for PCB manufacturing. These layout-level considerations are particularly important for minimizing unwanted reflections and losses that could otherwise degrade oscillation stability and phase noise.

The practical implementation plan also considers power delivery and biasing integrity across the PCB. Decoupling capacitors, bias routing, and ground plane continuity are selected to reduce supply noise and prevent coupling into RF-sensitive nodes. These considerations are guided by standard RF layout practices and are incorporated into the PCB design phase to ensure repeatable and stable operation during experimental testing.

Overall, this approach provides a systematic path toward technical demonstration. Each tool addresses a different layer of the design problem, allowing potential issues to be identified and mitigated early, thereby increasing the likelihood that the fabricated hardware will perform as intended during experimental validation.

4.2 Design Implementation

The design was developed with practical implementation in mind, with the goal of keeping the transition from simulation to hardware as straightforward as possible. To assess the different tuning strategies, simulations were carried out for both a varactor-based Colpitts oscillator and a midpoint biasing configuration.

A number of practical design considerations were taken into account. The biasing network is structured to supply a stable control voltage to the tuning node while maintaining isolation between RF nodes and low-frequency signals. This helps limit noise coupling from the control line and preserves the quality factor of the resonant tank, which is important for maintaining stable oscillation and low phase noise. The tuning voltage is applied through an op-amp buffer stage, providing a low output impedance and preventing unwanted loading of the control circuitry. In addition, parasitic elements such as series resistance and inductance are included in the model to better reflect non-ideal effects from component packaging, interconnects, and leads at gigahertz frequencies.

The simulation results highlight clear differences between the two approaches. Although the varactor-based configuration offers tunability in principle, it showed lower output power and less consistent oscillation in simulation. This behavior is likely due to the nonlinear characteristics and parasitic contributions of the varactor, which degrade the effective performance of the resonant tank at 5.4 GHz. In contrast, the midpoint biasing approach produced a stronger output signal and more stable oscillation, making it a more reliable option within the current design constraints.

4.3 Hardware Setup

The hardware validation of the proposed design is supported through a combination of circuit-level simulations and PCB implementation. To evaluate the effectiveness of the tuning approaches, two oscillator configurations were simulated in ADS: one incorporating a varactor diode and one using the midpoint biasing technique without a varactor.

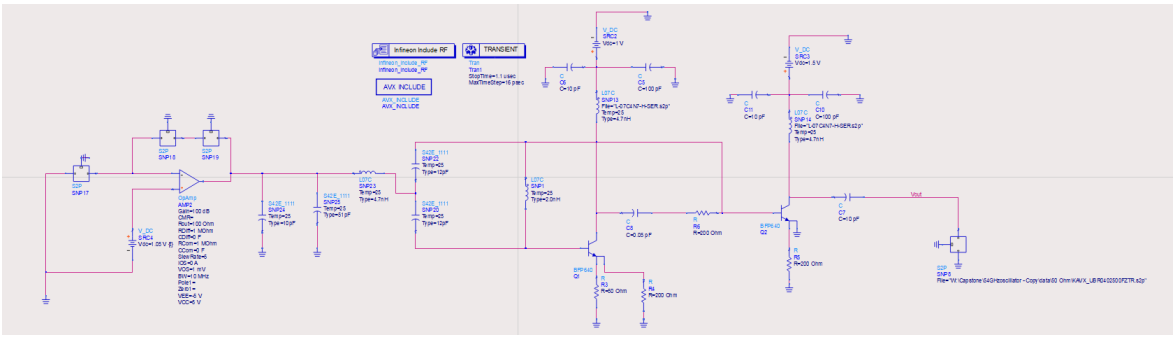

Figure 4.1: Colpitts oscillator configuration without varactor (midpoint tuning approach).

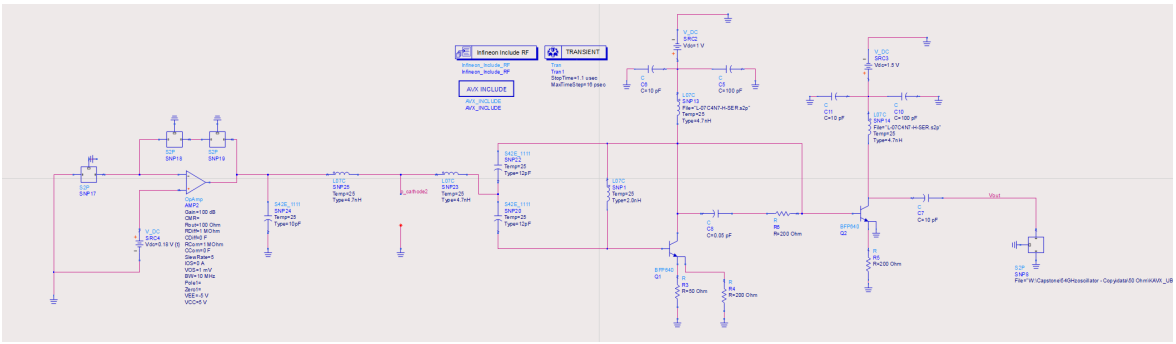

Figure 4.2: Colpitts oscillator configuration with varactor-based tuning.

Figures 4.1 and 4.2 show the two simulated oscillator configurations. In both cases, transient simulations were performed to observe steady-state oscillation behavior and output characteristics. The varactor-based design enables voltage-controlled tuning through its nonlinear capacitance, while the midpoint biasing approach applies a control voltage directly to the capacitive divider.

Simulation results showed a clear difference in performance between the two configurations. The varactor-based oscillator exhibited reduced output power and less stable oscillation, with greater sensitivity to bias conditions. This behavior is attributed to the nonlinear capacitance and parasitic elements of the varactor, which degrade the effective quality factor of the tank at 5.4 GHz. In contrast, the midpoint-tuned oscillator demonstrated a stronger and more stable output waveform, making it more suitable for practical implementation under the given constraints.

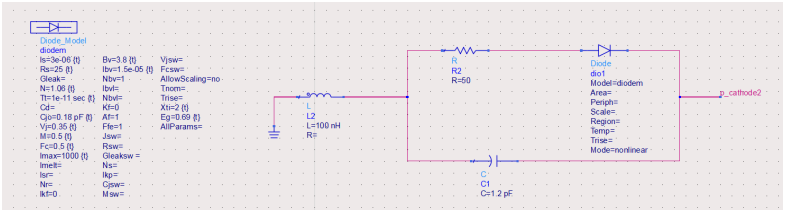

Figure 4.3: Varactor diode considered for tuning implementation.

Figure 4.3 shows the varactor device that was initially considered for implementation. Although this design works well as a varactor, integrating this into a stable high-frequency design requires careful modeling and biasing, which contributed to the decision to adopt the alternative tuning approach.

For the hardware implementation phase, responsibilities were divided between the project members. The oscillator PCB layout was designed by the project partner. This portion of the design focused on maintaining high quality factor, proper grounding, and minimizing parasitic effects at gigahertz frequencies. The op-amp control circuitry, which provides the tuning voltage to the oscillator, was designed separately.

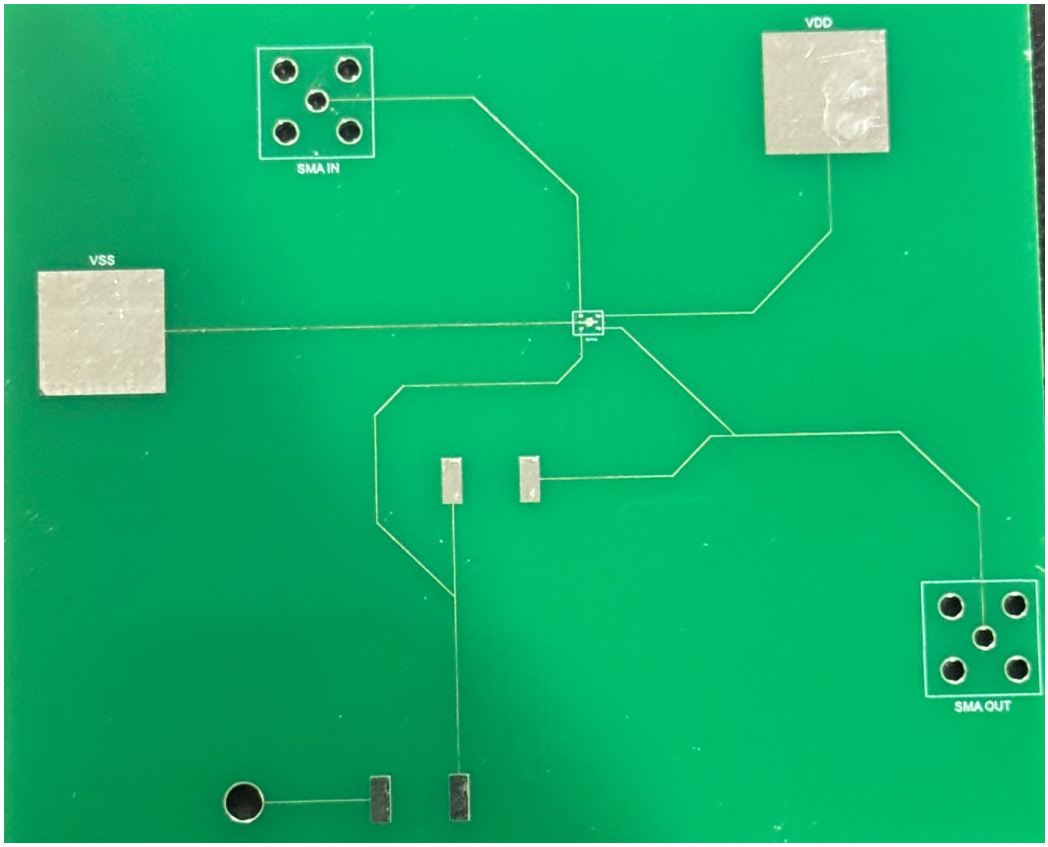

Figure 4.4: PCB layout of the op-amp.

Figure 4.4 shows the PCB layout of the op-amp section. Overall, the testing setup combines simulation-based verification with practical PCB design considerations. This approach allows performance differences between tuning methods to be clearly identified while ensuring that the final implementation remains feasible and robust for experimental validation.

4.4 Measurement Results

Simulation and experimental results were collected to evaluate the performance of the oscillator and op-amp tuning. The simulations focused on comparing the behavior of the Colpitts oscillator with and without a varactor, while the hardware tests verified the operation of the op-amp control stage and the oscillator output.

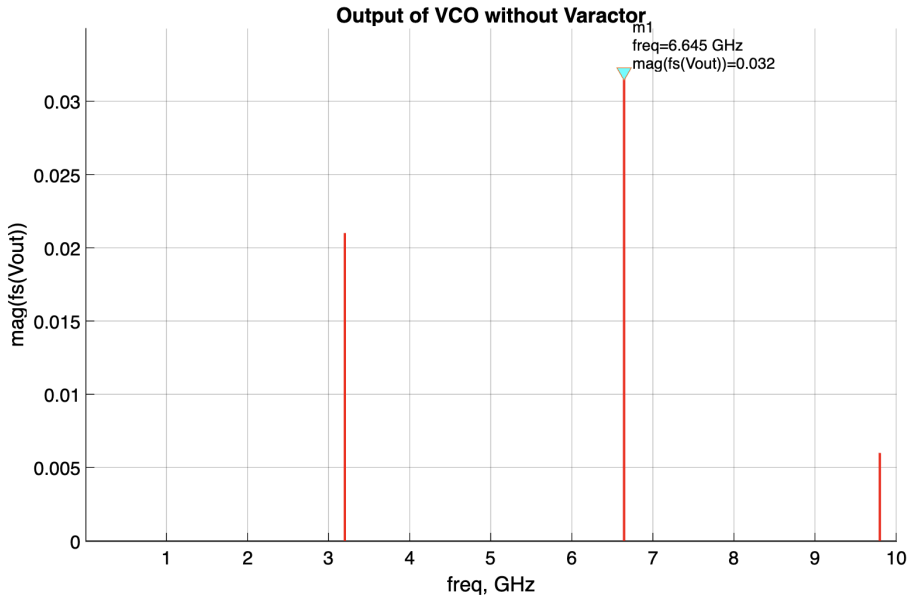

Figure 4.5: Simulated output of the Colpitts oscillator without varactor (midpoint tuning).

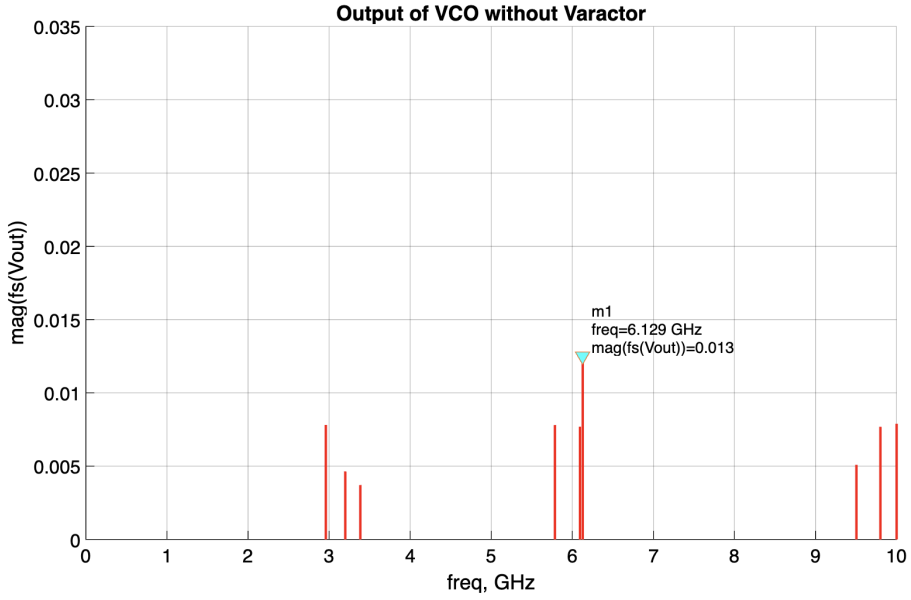

Figure 4.6: Simulated output of the Colpitts oscillator with varactor-based tuning.

Figures 4.5 and 4.6 show the simulated oscillator outputs. The configuration without the varactor shows a stable oscillation with consistent amplitude. Whereas, the varactor-based oscillator shows significantly lower output magnitude and contains numerous spikes and instabilities. This behavior is consistent with the nonlinearities and parasitic elements of the varactor, which degrade the tank's effective quality factor and reduce the overall output power.

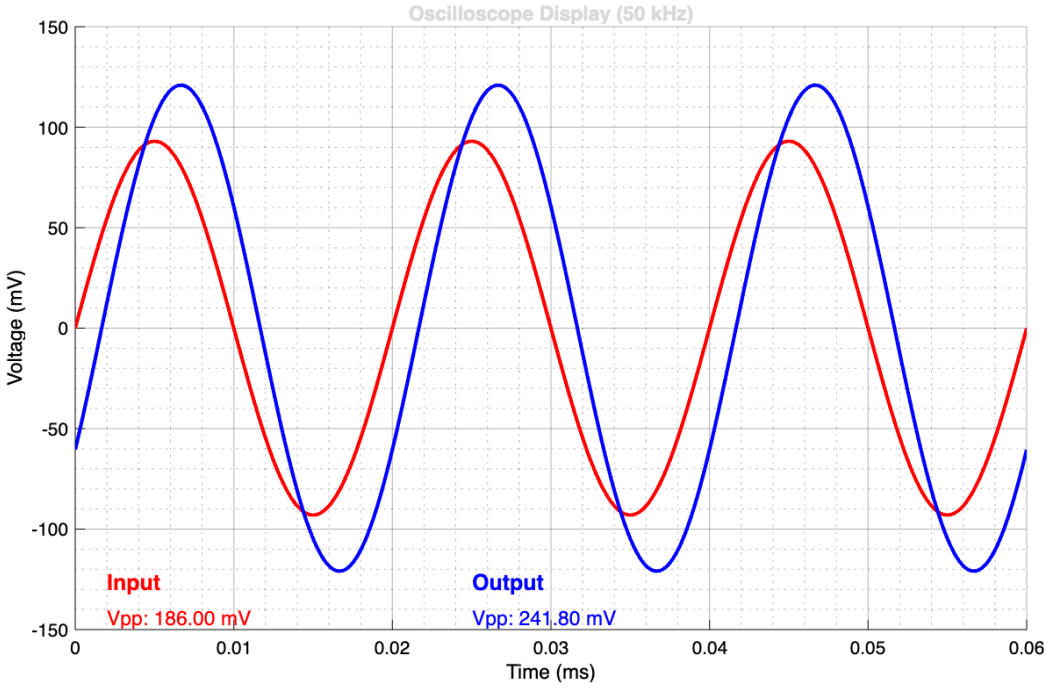

Figure 4.7: Measured output of the op-amp control circuit at 50 kHz.

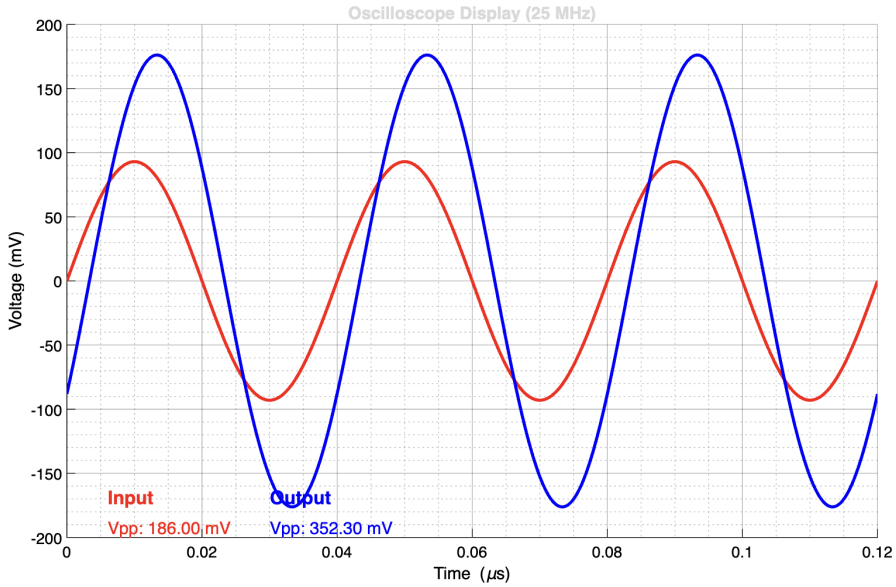

Figure 4.8: Measured output of the op-amp control circuit at 25 MHz.

Figures 4.7 and 4.8 present the measured outputs of the op-amp control circuit. The expected output is double the input, at 50 kHz, the output shows a much smaller expected output. At 25 MHz, the output is much cleaner, with the doubled waveform clearly resolved, confirming proper high-frequency operation of the control circuitry.

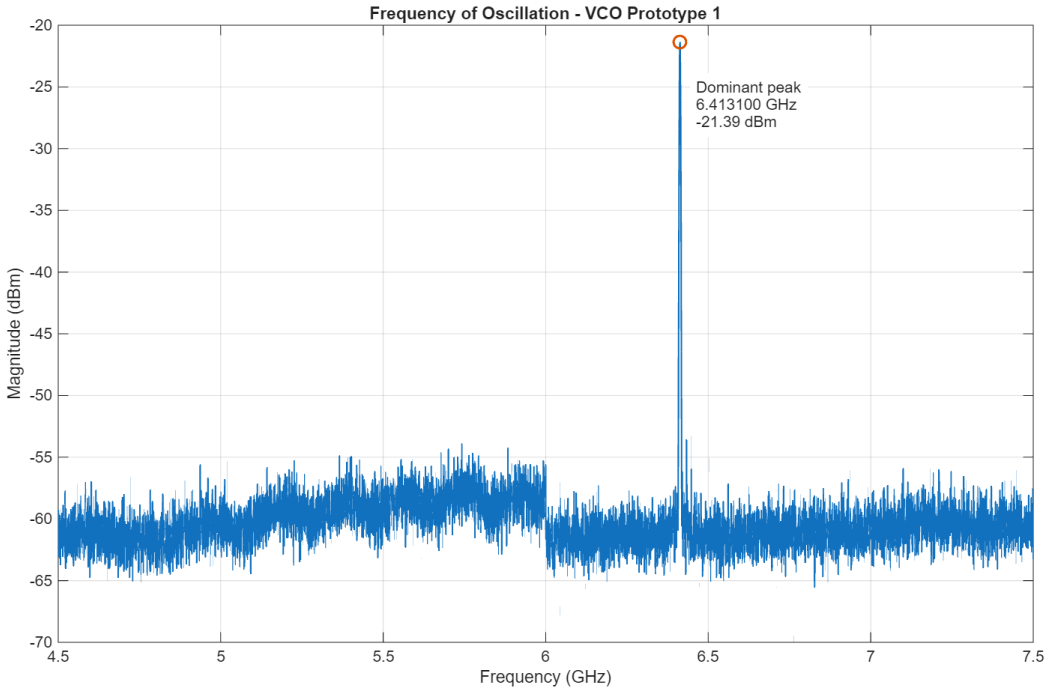

Figure 4.9: Measured output of the implemented Colpitts oscillator using midpoint tuning and op-amp control.

Figure 4.9 shows the measured output of the implemented oscillator. The results demonstrate stable oscillation with strong amplitude and minimal spiking, consistent with the simulation results of the midpoint tuning configuration. This validates the choice of the midpoint biasing approach and the effectiveness of the op-amp-based control voltage in maintaining stable operation.

4.5 Discussion

One major source of instability in the varactor-based oscillator is related to the difficulties in implementing the varactor device at 5.4 GHz. Potential mistakes in the varactor design include insufficient modeling of parasitic series resistance and package inductance, inaccurate biasing of the varactor diode, and improper selection of device capacitance relative to the tank circuit. These factors can reduce the effective quality factor of the LC tank, introduce nonlinearities, and cause spurious oscillations or amplitude fluctuations, which are consistent with the observed spikes and reduced output magnitude in simulation. Additionally, layout-dependent parasitics and coupling to nearby nodes may have further contributed to these instabilities, emphasizing the challenges of integrating varactor-based tuning at microwave frequencies[7;10].

Regarding the op-amp control circuit, measurements show that the BU7495HFV performs more effectively at higher frequencies (25 MHz) compared to lower frequencies (50 kHz). At low frequencies, the op-amp exhibits increased slew-rate limitations and greater susceptibility to low-frequency noise, which can distort the doubled output signal and reduce waveform fidelity. At higher frequencies, the op-amp operates within its intended high-speed regime, allowing the output to accurately reproduce fast transitions and maintain the expected doubling behavior[14;15]. This explains the cleaner waveform observed at 25 MHz and confirms the importance of matching op-amp bandwidth to the operating frequency of the control signal.

Finally, the oscillator simulations were performed at 6.6 GHz rather than the nominal 5.4 GHz to account for expected parasitic losses and layout-dependent detuning effects. At high frequencies, PCB trace parasitics, device packaging, and coupling can shift the resonant frequency of the LC tank. Simulating at a slightly higher frequency ensures that the realized oscillator will operate near the desired 5.4 GHz target once these real-world effects are considered, providing a more accurate prediction of hardware behavior[10;8].

Overall, these observations emphasize the importance of careful component selection, accurate modeling of high-frequency parasitics, and appropriate bandwidth considerations for both the oscillator and the control circuitry. While the varactor-based approach demonstrated theoretical tunability, practical limitations led to the selection of midpoint tuning with op-amp control, resulting in a more stable and robust implementation.

CHAPTER 5

CONCLUSIONS

5.1 Summary

The project focused on validating the tuning behavior of the Colpitts oscillator through numerical simulation and practical design considerations. Instead of a varactor-based approach, the oscillator was tuned using a midpoint biasing method combined with an op-amp control stage. Simulations confirmed that this configuration produces stable oscillation with strong output amplitude and predictable frequency adjustment, demonstrating superior performance compared to the varactor-based design, which exhibited lower output power and spurious spikes.

The op-amp control circuitry was experimentally verified at both low (50 kHz) and high (25 MHz) frequencies, showing that the high-frequency operation provides a cleaner and more accurate tuning signal. These results confirm the effectiveness of the op-amp in maintaining stable oscillator operation and mitigating susceptibility to control-line noise.

Overall, the midpoint-tuned oscillator with op-amp control provides a robust and practical solution for generating a stable frequency reference, supporting the broader goal of a tunable and reliable oscillator for the radar system. This work establishes a solid foundation for subsequent hardware implementation and experimental validation.

5.2 Overall Project Contributions and Achievements

The following points summarize my individual contributions and technical achievements throughout the project. These highlight specific challenges encountered, solutions applied, and the overall impact on the final oscillator design.

- **Design and Simulation of the Colpitts Oscillator**
  - Performed circuit-level simulations in ADS for both varactor-based and midpoint-biased oscillator configurations.
  - Investigated frequency tuning mechanisms and their impact on output amplitude and stability.
  - Identified critical issues with the varactor-based design, including reduced output power and spurious spikes due to parasitic capacitance and nonlinear behavior.
  - Analyzed the oscillator's response under varying control voltages to determine tuning range and sensitivity, providing insight into practical limitations.
  - Simulated high-frequency operation at 6.6 GHz to account for expected layout parasitics and signal loss, ensuring realistic prediction of the 5.4 GHz target performance.
- **Op-Amp Control Circuit Design**
  - Designed and implemented the op-amp-based tuning interface to deliver a stable control voltage to the midpoint of the oscillator capacitive divider.

  - Selected the BU7495HFV op-amp for its high-speed capabilities, low output impedance, and suitability for gigahertz-range oscillator control.
  - Performed experimental verification at both low (50 kHz) and high (25 MHz) frequencies, confirming cleaner signal doubling and better waveform fidelity at higher frequencies.
  - Integrated decoupling, bias routing, and grounding techniques to minimize noise coupling into RF-sensitive nodes.
  - Addressed technical challenges related to control-line noise and finite op-amp bandwidth, ensuring stable and predictable frequency tuning.

- **Evaluation and Comparison of Tuning Methods**
  - Compared varactor-based tuning against midpoint biasing with op-amp control using both simulation and analysis.
  - Demonstrated that the midpoint biasing approach achieves stronger and more stable output amplitude, with fewer spurious oscillations.
  - Provided clear justification for selecting the midpoint method based on practical implementability, stability, and hardware feasibility at 5.4 GHz.
  - Documented and analyzed the causes of varactor instability, including parasitic series resistance, package inductance, and non-ideal biasing.

- **PCB Layout and Practical Implementation Considerations**
  - Collaborated with project partner on PCB layout design, focusing on the LC tank, proper grounding, and minimizing parasitic effects at microwave frequencies.
  - Designed and tested the op-amp section layout, ensuring short trace lengths, decoupling capacitors, and continuity of the ground plane.
  - Applied standard RF layout practices to reduce unwanted reflections, losses, and coupling into RF nodes.
  - Ensured that the control voltage path was isolated from high-frequency RF oscillation paths, preserving the tank quality factor and phase noise performance.

- **Experimental Verification and Testing**
  - Conducted oscilloscope measurements of the op-amp output and the oscillator output to confirm simulation predictions.
  - Evaluated the impact of varying control voltages and verified that the midpoint biasing approach provides robust frequency control with minimal instability.
  - Documented discrepancies between varactor-based and midpoint-biased simulations to support the design decision.

- **Technical Problem-Solving and Project Management**
  - Identified technical challenges early in the simulation stage, including varactor nonlinearities, op-amp bandwidth limitations, and parasitic effects.
  - Proposed solutions such as midpoint biasing, op-amp buffering, and high-frequency simulation adjustments to mitigate potential issues.
  - Ensured the integration of simulation, PCB layout, and experimental testing in a systematic workflow.
  - Provided technical documentation, figure generation, and discussion content for the report, linking all experimental and simulation results to project objectives.

- **Contribution to Overall Project Outcome**

  - My work on the op-amp design and tuning interface enabled stable frequency control for the oscillator, a critical requirement for the radar system's phase-locked loop operation.
  - By evaluating both tuning approaches and identifying the practical limitations of varactor implementation, I contributed to a more robust and implementable final design.
  - The combined efforts of simulation, design, and experimental validation provided confidence that the oscillator can deliver a stable, tunable 5.4 GHz frequency reference for the system.
  - Overall, my contributions ensured that the project objectives were met efficiently while addressing technical challenges with practical solutions.

5.3 Future Work

While the current phase of the project successfully demonstrated a stable and tunable 5.4 GHz Colpitts oscillator using the midpoint biasing approach and op-amp control circuitry, several critical areas remain for improvement and further development. These areas represent opportunities for future work to enhance oscillator performance, reduce instabilities, and improve experimental control.

- **Varactor-Based Oscillator Implementation**
  - Although the varactor-based tuning approach was initially considered, practical difficulties in its implementation prevented its use in the current design.
  - Future work should focus on designing or selecting a high-performance varactor with low series resistance, minimal parasitic inductance, and appropriate capacitance range for a 5.4 GHz LC tank.
  - Detailed modeling of the varactor, including layout-dependent parasitics and package effects, should be conducted to accurately predict oscillator behavior.
  - A carefully implemented varactor-based oscillator would provide more precise voltage-controlled frequency tuning, improved linearity, and potentially lower phase noise compared to the midpoint biasing approach.
  - Experimental testing should be performed to validate simulation predictions, optimize biasing networks, and minimize spurious oscillations.
  - Additionally, exploring temperature-compensated or graded varactors could further improve oscillator stability and robustness in varying environmental conditions.
- **Custom Op-Amp Design**
  - In the current design, the BU7495HFV op-amp was used to deliver the tuning voltage to the oscillator. While effective, the datasheet does not provide complete information about internal transistor-level parameters and parasitic elements, limiting the accuracy of high-frequency testing and simulation.
  - A possible future improvement is to design a custom op-amp tailored for the oscillator control interface. This would allow complete control over all components and their values, enabling more precise tuning of bandwidth, slew rate, noise performance, and output impedance.
  - A custom op-amp would also allow for optimization of stability and response speed at gigahertz-range control signals, further enhancing the oscillator's performance under high-frequency operation.
  - Integration of on-chip decoupling and filtering could be implemented in the custom design to minimize susceptibility to power-supply and control-line noise.
  - Experimental verification could then be performed with full confidence that all circuit parameters are known and characterized, providing a more accurate evaluation of the oscillator's phase noise, tuning linearity, and amplitude stability.
- **High-Frequency PCB and Layout Optimization**
  - Future work should also include more detailed optimization of PCB layout for both the oscillator and op-amp control sections.

  - Incorporating electromagnetic simulations for all layout traces, interconnects, and grounding strategies would help predict and mitigate parasitic effects, crosstalk, and unintended resonances at 5.4 GHz.
  - Exploration of multi-layer PCB designs with controlled impedance traces and improved isolation between RF and control paths could further improve oscillator stability.
  - This layout optimization would be especially beneficial if a varactor-based design is implemented, as varactor non-linearities are more sensitive to parasitic loading.

- **Advanced Measurement and Characterization**

  - Future work could include more detailed experimental characterization of both the oscillator and the op-amp control circuits.
  - This could involve phase-noise measurement, frequency spectrum analysis under different bias conditions, and temperature variation testing.
  - Characterization of the op-amp performance at higher frequencies using signal analyzers could validate the expected clean doubling behavior across the full tuning range.
  - Comparisons with simulation results would help refine models, improve component selection, and identify previously unaccounted-for parasitic effects.

- **Integration with Full Radar System**

  - The ultimate goal of this project is to provide a tunable and stable frequency reference for a radar system.
  - Future work could focus on integrating the oscillator and control circuitry into a full system, evaluating performance under realistic operating conditions.
  - This would include examining phase-locked loop behavior, frequency stability, and overall system-level noise contributions.
  - Optimizing the oscillator and op-amp for integration would ensure that the design improvements, such as a working varactor and custom op-amp, directly translate to enhanced radar performance.

Overall, these future directions aim to address the critical shortcomings identified in the current design, particularly the limitations of varactor implementation and reliance on off-the-shelf op-amps. By working more thoroughly to develop a high-performance varactor and designing a custom op-amp, the oscillator system could achieve improved tuning accuracy, output stability, and robustness under high-frequency operation. These enhancements would provide a stronger foundation for both experimental validation and integration into advanced radar applications.

CHAPTER 6

APPENDIX

6.1 Extension from Fall Work Term

Fall Term Work

In the Fall term, the main focus was on modeling the varactor and verifying its tuning behavior. An HSPICE model was created using datasheet parameters and implemented in ADS. By sweeping the reverse-bias voltage, the capacitance–voltage relationship was extracted and compared to expected theoretical behavior.

This showed that the varactor model behaved correctly and could be used for tuning purposes. However, the work at this stage was limited to the device level. The varactor was not yet integrated into a full oscillator, and there was no hardware implementation. Parasitics were only partially considered, and system-level effects like oscillation stability and output amplitude were not analyzed.

Winter Term Work and Extensions

In the Winter term, the work was extended significantly by moving from just modeling the varactor to actually building and testing a full oscillator system.

Integration into the Colpitts Oscillator

The first major step was integrating the tuning method into a Colpitts oscillator. This made it possible to evaluate how the tuning mechanism affects real oscillator behavior, such as frequency, amplitude, and stability. This is a key difference from the Fall term, where only the varactor itself was studied.

Issues with the Varactor-Based Design

Once the varactor was added to the oscillator, several issues became clear. The output amplitude was much lower than expected, and the waveform showed instability and spikes. These problems were mainly due to parasitic effects and the nonlinear behavior of the varactor at high frequencies.

This was an important result, because even though the varactor worked correctly in simulation during the Fall term, it did not perform well when used in the full oscillator. This showed that validating a component alone is not enough for a high-frequency system.

Alternative Tuning Method

Because of these issues, a different tuning approach was explored. Instead of using a varactor, midpoint biasing was implemented by applying the control voltage directly to the capacitive divider.

This approach gave much better results in simulation. The oscillator had a stronger output and was much more stable. Based on this comparison, the midpoint tuning method was chosen for the final design since it was simpler and more reliable.

Op-Amp Control Circuit

An op-amp circuit was designed to provide the tuning voltage. The goal was to buffer the control signal and avoid loading the oscillator.

Testing showed that the op-amp performance depended heavily on frequency. At 50 kHz, the output was noisy and distorted, while at 25 MHz the signal was much cleaner. This highlighted the importance of choosing components that match the operating frequency of the system.

PCB Design and Hardware Work

Another major extension from the Fall term was the move to hardware. The op-amp circuit was implemented on a PCB, and the oscillator layout was developed as part of the group work.

This introduced practical challenges that were not present in simulation, such as layout parasitics, grounding, and noise coupling. Standard RF design practices like decoupling and short trace routing were used to improve performance.

Experimental Testing

Measurements were taken using an oscilloscope to verify both the op-amp and oscillator performance. The midpoint-tuned oscillator showed stable oscillation with good amplitude, which matched the simulation results.

This is a major improvement compared to the Fall term, where no experimental validation was done.

High-Frequency Adjustments

To account for parasitic effects in hardware, the oscillator was simulated at 6.6 GHz instead of 5.4 GHz. This helps ensure that the final built circuit operates closer to the desired frequency after real-world losses are included.

Key Differences Between Fall and Winter Work

- Fall work focused on varactor modeling, while Winter work focused on full oscillator design
- Fall simulations were mostly ideal, while Winter work included parasitic and layout effects
- No hardware was built in the Fall, while Winter included PCB design and testing
- The varactor approach was assumed to work in the Fall, but was later shown to have practical issues
- Winter work included op-amp design and integration, which was not part of the Fall work

Overall Progress

Overall, the project progressed from a basic simulation of a tuning component to a working oscillator design that was tested in hardware. The Winter term work showed the importance of considering real-world effects and adapting the design when initial approaches do not perform as expected. The final result is a more practical and stable tuning method that can be used in the PLL system.

6.2 Project Resources

This section provides the necessary circuit diagrams, PCB layouts, and testing equipment required to reproduce the work presented in this report.

The following figures show the key circuit designs used throughout the project, including the oscillator and control circuitry.

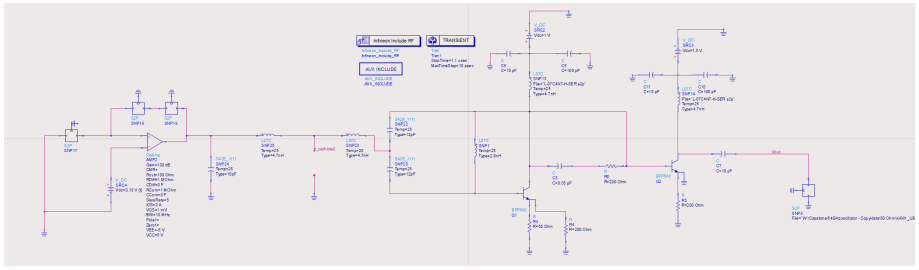

Figure 6.1: Colpitts oscillator schematic with Varactor

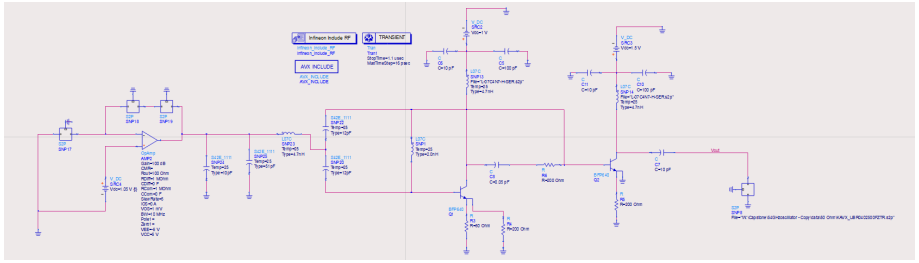

Figure 6.2: Colpitts oscillator schematic without Varactor

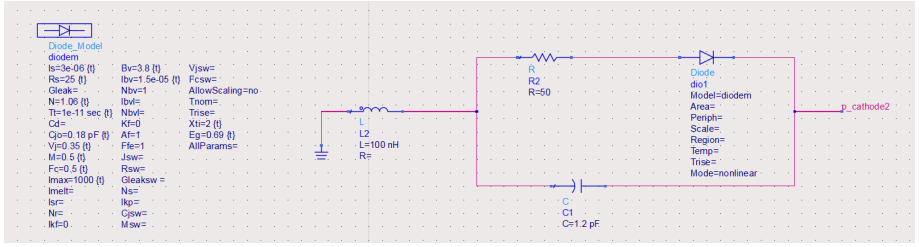

Figure 6.3: The tested varactor design

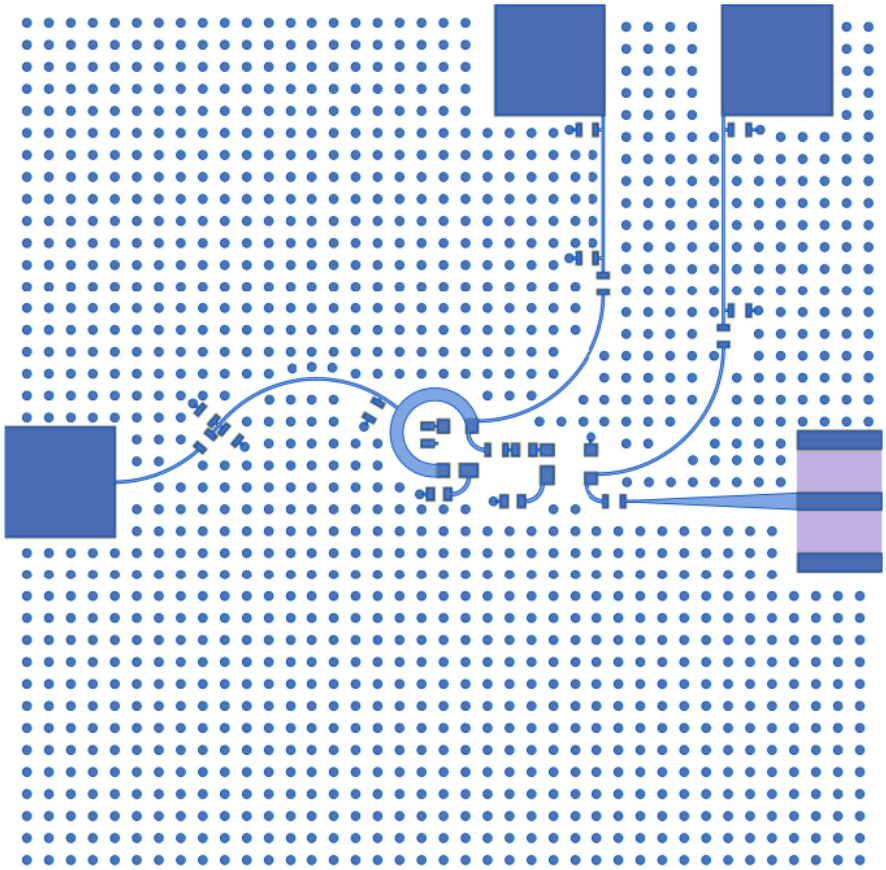

Figure 6.4: Oscillator PCB layout

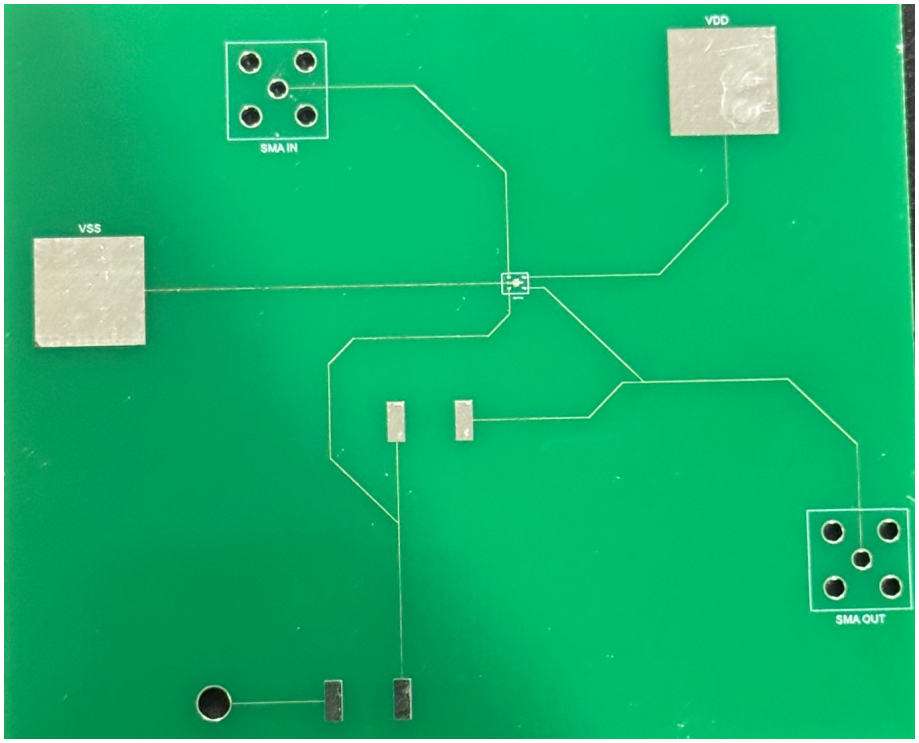

Figure 6.5: Op-amp PCB layout

The following equipment was used for testing and validation:

- Oscilloscope

- Signal generator
- DC power supply

The following is the Matlab script used to create better graphs from simulated date:

```
clear; clc; close all;

data = readmatrix('vco_spectrum.csv');

freq = data(:,1);
mag  = data(:,2);

%% Create figure
figure('Color','w');
h = axes;
set(h,'Color','w');
hold on;

stem(freq, mag, 'r', 'LineWidth', 1.5, 'Marker','none');

grid on;
set(h, 'XColor','k', 'YColor','k', 'GridColor','k', 'MinorGridColor','k', '
    FontSize',12);

xlabel('freq, GHz', 'Color','k');
ylabel('mag(fs(Vout))', 'Color','k');
title('Output of VCO without Varactor', 'Color','k');

xlim([0 10]);
ylim([0 0.035]);

[peak_val, idx] = max(mag);

plot(freq(idx), peak_val, 'v', 'MarkerFaceColor', 'c', 'MarkerSize', 8);

text(freq(idx), peak_val, ...
    sprintf('  m1\n  freq=%.3f GHz\n  mag(fs(Vout))=%.3f', ...
    freq(idx), peak_val), ...
    'VerticalAlignment','bottom', ...
    'Color','k');

hold off;
```

BIBLIOGRAPHY

[1] Federal Aviation Administration, "Unmanned aircraft systems (uas) integration and operational concepts," FAA, 2020, online resource.

[2] NASA, "Uas traffic management (utm)," National Aeronautics and Space Administration, 2019, online program overview.

[3] M. I. Skolnik, *Radar Handbook*, 3rd ed. New York, NY, USA: McGraw-Hill, 2008.

[4] M. A. Richards, *Fundamentals of Radar Signal Processing*, 2nd ed. New York, NY, USA: McGraw-Hill Education, 2014.

[5] A. Blanchard, *Phase-Locked Loops: Application to Coherent Receiver Systems*. New York, NY, USA: John Wiley & Sons, 1976.

[6] F. M. Gardner, *Phaselock Techniques*, 3rd ed. Hoboken, NJ, USA: John Wiley & Sons, 2005.

[7] L. Dai and R. Harjani, *Design of High-Performance CMOS Voltage-Controlled Oscillators*. Boston, MA, USA: Springer, 2003.

[8] B. Razavi, "A study of phase noise in LC oscillators," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 3, pp. 331–343, 1996.

[9] R. E. Best, *Phase-Locked Loops: Design, Simulation, and Applications*, 6th ed. New York, NY, USA: McGraw-Hill, 2007.

[10] D. M. Pozar, *Microwave Engineering*, 4th ed. Hoboken, NJ, USA: Wiley, 2012.

[11] "SMV1405 to SMV1430 Series: Plastic-Packaged Abrupt Junction Tuning Varactors Datasheet," Online datasheet, Mouser Electronics / Skyworks Solutions Inc., Skyworks Solutions, Inc., 2020, available: https://www.mouser.ca/datasheet/3/564/1/SMV1405_1430_Series_200068W.pdf.

[12] Keysight Technologies, *Advanced Design System (ADS) Documentation*, Keysight Technologies, 2024, online documentation.

[13] Texas Instruments, "Voltage-controlled oscillator design considerations," Application Note, 2016, available online.

[14] *BU7495HFV High-Speed Operational Amplifier Datasheet*, Rohm Semiconductor, 2019, available online at https://www.rohm.com/datasheet/bu7495hfv.

[15] S. Franco, *Design with Operational Amplifiers and Analog Integrated Circuits*, 4th ed. McGraw-Hill, 2015.